EAST SEARCH

4/11/04

L#	Hits	Search String	Databases
L1	6	(("6629312") or ("6457173") or ("6490716")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	1	5355491.PN.	USPAT
L3	1	6226776.PN.	USPAT
L4	1	6292938.PN.	USPAT
L5	1	6463582.PN.	USPAT
L6	1	6226776.PN.	USPAT
L7	1	6279100.PN.	USPAT
L8	5	(vliw or (very adj long adj instruction)) same (mutual$4 and exclusiv$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	148	(vliw or (very adj long adj instruction)) and (mutual$4 and exclusiv$5) and parallel$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L8:

US 6604188 B1	Pipeline replay support for multi-cycle operations wherein all VLIW instructions are flushed upon detection of a multi-cycle atom operation in a VLIW instruction	20030805	712/24
US 6457173 B1	Automatic design of VLIW instruction formats	20020924	717/149
US 5974537 A	Guard bits in a VLIW instruction control routing of operations to functional units allowing two issue slots to specify the same functional unit	19991026	712/215
US 5333280 A	Parallel pipelined instruction processing system for very long instruction word	19940726	712/241
JP 2001306321 A	Processor of very long instruction word system, has primary and secondary conditions which are not mutually exclusive relationships	20011102	

Results of search set L9:

US 6702417 B2	Printing cartridge with capacitive sensor identification	20040309	347/19
US 6697076 B1	Method and apparatus for address re-mapping	20040224	345/568
US 6693643 B1	Method and apparatus for color space conversion	20040217	345/602
US 6675286 B1	Multimedia instruction set for wide data paths	20040106	712/215
US 6665454 B1	Dot adjacency compensation in optical storage systems using ink dots	20031216	382/299
US 6651222 B2	Automatic design of VLIW processors	20031118	716/1
US 6644771 B1	Printing cartridge with radio frequency identification	20031111	347/19
US 6643745 B1	Method and apparatus for prefetching data into cache	20031104	711/138

US 6636216 B1	Digital image warping system	20031021	345/427
US 6631514 B1	Emulation system that uses dynamic binary translation and permits the safe speculation of trapping operations	20031007	717/137
US 6629312 B1	Programmatic synthesis of a machine description for retargeting a compiler	20030930	717/136
US 6629001 B1	Configurable controller for audio channels	20030930	700/94
US 6618117 B2	Image sensing apparatus including a microcontroller	20030909	355/18
US 6607888 B2	Method for analyzing nucleic acid reactions	20030819	435/6
US 6604188 B1	Pipeline replay support for multi-cycle operations wherein all VLIW instructions are flushed upon detection of a multi-cycle atom operation in a VLIW instruction	20030805	712/24
US 6588009 B1	Method and apparatus for compiling source code using symbolic execution	20030701	717/161
US 6587058 B1	Processing circuit and method for variable-length coding and decoding	20030701	341/67
US 6581191 B1	Hardware debugging in a hardware description language	20030617	716/4
US 6581187 B2	Automatic design of VLIW processors	20030617	716/1
US 6573846 B1	Method and apparatus for variable length decoding and encoding of video streams	20030603	341/67
US 6565181 B2	Printing cartridge with switch array identification	20030520	347/19
US 6549930 B1	Method for scheduling threads in a multithreaded processor	20030415	718/104
US 6547364 B2	Printing cartridge with an integrated circuit device	20030415	347/19
US 6542645 B1	Adaptive tracking of dots in optical storage system using ink dots	20030401	382/254
US 6539543 B1	Method and apparatus for compiling source code by flattening hierarchies	20030325	717/161
US 6507947 B1	Programmatic synthesis of processor element arrays	20030114	717/160
US 6507293 B2	Processing circuit and method for variable-length coding and decoding	20030114	341/67
US 6496919 B1	Data processor	20021217	712/24
US 6490716 B1	Automated design of processor instruction units	20021203	716/18
US 6476863 B1	Image transformation means including user interface	20021105	348/231.9
US 6459495 B1	Dot center tracking in optical storage systems using ink dots	20021001	358/520
US 6457173 B1	Automatic design of VLIW instruction formats	20020924	717/149
US 6457073 B2	Methods and apparatus for providing data transfer control	20020924	710/22
US 6445316 B1	Universal impedance control for wide range loaded signals	20020903	341/120
US 6442525 B1	System for authenticating physical objects	20020827	705/1
US 6438747 B1	Programmatic iteration scheduling for parallel processors	20020820	717/160
US 6431669 B1	Method and apparatus for information storage in a portable print roll	20020813	347/2
US 6416154 B1	Printing cartridge with two dimensional code identification	20020709	347/19
US 6415054 B1	Target detection for dot region alignment in optical storage systems using ink dots	20020702	382/233
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candidate systems	20020618	716/17
US 6397242 B1	Virtualization system including a virtual machine monitor for a computer with a segmented architecture	20020528	718/1
US 6385757 B1	Auto design of VLIW processors	20020507	716/1

US 6380758 B1	Impedance control for wide range loaded signals using distributed methodology	20020430	326/30
US 6374403 B1	Programmatic method for reducing cost of control in parallel processes	20020416	717/161
US 6374346 B1	Processor with conditional execution of every instruction	20020416	712/221
US 6362869 B1	Authentication system for camera print rolls	20020326	355/18
US 6362868 B1	Print media roll and ink replaceable cartridge	20020326	355/18
US 6356715 B1	Prints remaining indicating for camera with variable length print capability	20020312	396/284
US 6356105 B1	Impedance control system for a center tapped termination bus	20020312	326/30
US 6351760 B1	Division unit in a processor using a piece-wise quadratic approximation technique	20020226	708/654
US 6321322 B1	Methods and apparatus for scalable instruction set architecture with dynamic compact instructions	20011120	712/24
US 6317192 B1	Utilization of image tiling effects in photographs	20011113	355/18
US 6315200 B1	Encoded data card reading system	20011113	235/454
US 6314511 B1	Mechanism for freeing registers on processors that perform dynamic out-of-order execution of instructions using renaming registers	20011106	712/217
US 6298370 B1	Computer operating process allocating tasks between first and second processors at run time based upon current processor load	20011002	718/102
US 6282708 B1	Method and processor for structuring a multi-instruction computer program in an internal directed acyclic graph	20010828	717/156
US 6282632 B1	Information processor having duplicate operation flags	20010828	712/42
US 6260082 B1	Methods and apparatus for providing data transfer control	20010710	710/22
US 6221592 B1	Computer-based methods and systems for sequencing of individual nucleic acid molecules	20010424	435/6
US 6217165 B1	Ink and media cartridge with axial ink chambers	20010417	347/86
US 6202143 B1	System for fetching unit instructions and multi instructions from memories of different bit widths and converting unit instructions to multi instructions by adding NOP instructions	20010313	712/210
US 6195748 B1	Apparatus for sampling instruction execution information in a processor pipeline	20010227	712/227
US 6182203 B1	Microprocessor	20010130	712/22
US 6179489 B1	Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto	20010130	718/102
US 6163840 A	Method and apparatus for sampling multiple potentially concurrent instructions in a processor pipeline	20001219	712/227
US 6148396 A	Apparatus for sampling path history in a processor pipeline	20001114	712/227
US 6119075 A	Method for estimating statistics of properties of interactions processed by a processor pipeline	20000912	702/186
US 6112298 A	Method for managing an instruction execution pipeline during debugging of a data processing system	20000829	712/227

US 6105119 A	Data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems	20000815	711/219
US 6092184 A	Parallel processing of pipelined instructions having register dependencies	20000718	712/218
US 6092180 A	Method for measuring latencies by randomly selected sampling of the instructions while the instruction are executed	20000718	712/200
US 6081885 A	Method and apparatus for halting a processor and providing state visibility on a pipeline phase basis	20000627	712/227
US 6070009 A	Method for estimating execution rates of program execution paths	20000530	717/130
US 6065106 A	Resuming normal execution by restoring without refetching instructions in multi-word instruction register interrupted by debug instructions loading and processing	20000516	712/24
US 6055649 A	Processor test port with scan chains and data streaming	20000425	714/30
US 6023757 A	Data processor	20000208	712/209
US 6016555 A	Non-intrusive software breakpoints in a processor instruction execution pipeline	20000118	714/35
US 6000044 A	Apparatus for randomly sampling instructions in a processor pipeline	19991207	714/47
US 5983336 A	Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups	19991109	712/24
US 5974537 A	Guard bits in a VLIW instruction control routing of operations to functional units allowing two issue slots to specify the same functional unit	19991026	712/215
US 5970241 A	Maintaining synchronism between a processor pipeline and subsystem pipelines during debugging of a data processing system	19991019	712/227
US 5968160 A	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	19991019	712/14
US 5964867 A	Method for inserting memory prefetch operations based on measured latencies in a program optimizer	19991012	712/219
US 5949994 A	Dedicated context-cycling computer with timed context	19990907	712/228
US 5949439 A	Computing apparatus and operating method using software queues to improve graphics performance	19990907	345/503
US 5924117 A	Multi-ported and interleaved cache memory supporting multiple simultaneous accesses thereto	19990713	711/127
US 5923872 A	Apparatus for sampling instruction operand or result values in a processor pipeline	19990713	712/244
US 5923871 A	Multifunctional execution unit having independently operable adder and multiplier	19990713	712/221
US 5909559 A	Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width	19990601	710/307
US 5890217 A	Coherence apparatus for cache of multiprocessor	19990330	711/141
US 5883640 A	Computing apparatus and operating method using string caching to improve graphics performance	19990316	345/503

US 5809450 A	Method for estimating statistics of properties of instructions processed by a processor pipeline	19980915	702/186
US 5790874 A	Information processing apparatus for reducing power consumption by minimizing hamming distance between consecutive instruction	19980804	713/320
US 5787026 A	Method and apparatus for providing memory access in a processor pipeline	19980728	708/521
US 5784630 A	Method and apparatus for processing data in multiple modes in accordance with parallelism of program by using cache memory	19980721	712/30
US 5764951 A	Methods for automatically pipelining loops	19980609	716/1
US 5764943 A	Data path circuitry for processor having multiple instruction pipelines	19980609	712/218
US 5699460 A	Image compression coprocessor with data flow control and multiple processing units	19971216	382/307
US 5682491 A	Selective processing and routing of results among processors controlled by decoding instructions using mask value derived from instruction tag and processor identifier	19971028	712/209
US 5471593 A	Computer processor with an efficient means of executing many instructions simultaneously	19951128	712/235
US 5450556 A	VLIW processor which uses path information generated by a branch control unit to inhibit operations which are not on a correct path	19950912	712/235
US 5442760 A	Decoded instruction cache architecture with each instruction field in multiple-instruction cache line directly connected to specific functional unit	19950815	712/215
US 5333280 A	Parallel pipelined instruction processing system for very long instruction word	19940726	712/241
US 5329630 A	System and method using double-buffer preview mode	19940712	711/173
US 5056015 A	Architectures for serial or parallel loading of writable control store	19911008	703/27
US 4873630 A	Scientific processor to support a host processor referencing common memory	19891010	712/3
US 20040065738 A1	Data distribution mechanism in the form of ink dots on cards	20040408	235/454
US 20040061734 A1	Printing device for use with a printing cartridge having capacitive sensor identification	20040401	347/19
US 20040056105 A1	Data structure encoded on a surface of an object	20040325	235/494
US 20040051753 A1	Method of identifying printing cartridge characteristics with capacitive sensors	20040318	347/19
US 20040041018 A1	Card having coded data and visible information, for operating a device	20040304	235/375
US 20040030873 A1	Single chip multiprocessing microprocessor having synchronization register file	20040212	712/245
US 20040015931 A1	Methods and apparatus for automated generation of abbreviated instruction set and configurable processor architecture	20040122	717/158
US 20040015773 A1	High speed arithmetic operations for use in turbo decoders	20040122	714/786
US 20040008327 A1	Image printing apparatus including a microcontroller	20040115	355/18
US 20040008262 A1	Utilization of color transformation effects in photographs	20040115	348/207.2
US 20040008261 A1	Print roll for use in a camera imaging system	20040115	348/207.2
US 20040004698 A1	Programmable camera system with software interpreter	20040108	355/18

US 20040004651 A1	Printing cartridge with a data-carrying integrated circuit device	20040108	347/86
US 20040004129 A1	Identifying card	20040108	235/487
US 20030233642 A1	System and method for assigning basic blocks to computer control flow paths	20031218	717/156
US 20030233641 A1	System and method for merging control flow paths	20031218	717/156
US 20030200420 A1	Methods and apparatus for scalable instruction set architecture with dynamic compact instructions	20031023	712/209
US 20030126404 A1	Data processing system, array-type processor, data processor, and information storage medium	20030703	712/15
US 20030120996 A1	High speed add-compare-select operations for use in viterbi decoders	20030626	714/795
US 20030117496 A1	Preprinted print rolls for postal use in an image processing device	20030626	348/207.2
US 20030112419 A1	Printing cartridge with barcode identification	20030619	355/18
US 20030079065 A1	Methods and apparatus for providing data transfer control	20030424	710/22
US 20030068185 A1	Printing cartridge with switch array identification	20030410	400/613
US 20030066061 A1	Method and apparatus for performing compiler transformation of software code using fastforward regions and value specialization	20030403	717/158
US 20030065911 A1	Data processor	20030403	712/227
US 20030056088 A1	Processor, compiler and compilation method	20030320	712/214
US 20030041163 A1	Data processing architectures	20030227	709/232
US 20030033441 A1	HIGHLY COMPONENTIZED SYSTEM ARCHITECTURE WITH A DEMAND-LOADING NAMESPACE AND PROGRAMMING MODEL	20030213	719/315
US 20020144101 A1	Caching DAG traces	20021003	712/240
US 20020133784 A1	Automatic design of VLIW processors	20020919	716/1
US 20020120914 A1	Automatic design of VLIW processors	20020829	716/17
US 20020083308 A1	Data processing device with a configurable functional unit	20020627	712/226
US 20020080335 A1	Printing cartridge with capacitive sensor identification	20020627	355/18
US 20020073299 A1	Methods and apparatus for scalable instruction set architecture with dynamic compact instructions	20020613	712/24
US 20020071104 A1	Image sensing apparatus including a microcontroller	20020613	355/18
US 20020061523 A1	Method for analyzing nucleic acid reactions	20020523	435/6
US 20020033854 A1	Printing cartridge with pressure sensor array identification	20020321	347/17
US 20020030713 A1	Printing cartridge with two dimensional code identification	20020314	347/19
US 20020030712 A1	Printing cartridge with an integrated circuit device	20020314	347/19
US 20020011943 A1	Processing circuit and method for variable-length coding and decoding	20020131	341/67
US 20020010814 A1	Methods and apparatus for providing data transfer control	20020124	710/22
US 20010004755 A1	MECHANISM FOR FREEING REGISTERS ON PROCESSORS THAT PERFORM DYNAMIC OUT-OF-ORDER EXECUTION OF INSTRUCTIONS USING RENAMING REGISTERS	20010621	712/217